A Miniature Broad-Band pHEMT MMIC Balanced Distributed Doubler

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***Abstract*—A miniature broad-band balanced frequency doubler has been designed to operate from 30 to 50 GHz. It comprises a reduced-size 180° rat-race hybrid and two distributed doublers to form a balanced doubler configuration. The balanced distributed doubler suppresses the 180° out-of-phase fundamental and third harmonic signals at the output port while combining the in-phase second harmonic signal. A measured conversion loss of 5–7 dB from 30- to 50-GHz output frequencies is achieved with fundamental and third harmonic signals rejection better than 13 and 25 dB, respectively. The chip size is only 1.5×1 mm^2.**

***Index Terms*—Balanced doublers, distributed doublers, monolithic microwave integrated circuit (MMIC), reduced-size rat-race.**

I. Introduction

THE increasing demand for millimeter-wave (MMW) wireless communication systems has raised the necessity to realize high-quality MMW sources. Since there are difficulties to implement fundamental frequency oscillators in the MMW regime with low phase noise, the low-frequency oscillator cascade with frequency multipliers approach is still very popular for extreme low phase-noise MMW sources. Most of reported frequency multipliers are narrow-band single-ended designs implemented either with diodes or FETs [1]–[4]. However, broad-band frequency multipliers are needed for wide-bandwidth applications. A balanced doubler approach for frequency can easily achieve good fundamental and odd-harmonics rejections [5]. A couple of broad-band frequency doublers have been reported using common-source/common-drain FET configuration with balanced doubler structures [6]–[9] up to 40-GHz output frequency. Distributed doublers, which have the potential for MMW frequency ranges were also published using diodes [10]–[12]. A balanced distributed monolithic-microwave integrated-circuit (MMIC) doubler implemented using common-gate/common-source FETs to achieve 180° out-of-phase characteristics at input and, thus, for balanced doubler operations from 10- to 18-GHz output frequency [13]. The operation frequency of this approach is limited by the antiphasal characteristic of common-gate/common-source FETs. For the MMW frequency, a balanced V-band doubler that employs a balun and two single-ended doublers with common-source high electron-mobility transistors (HEMTs) were reported [14]. In order to have a wide-band operation at a higher frequency, using a broad-band balun with distributed FET doublers seems to be an attractive approach.

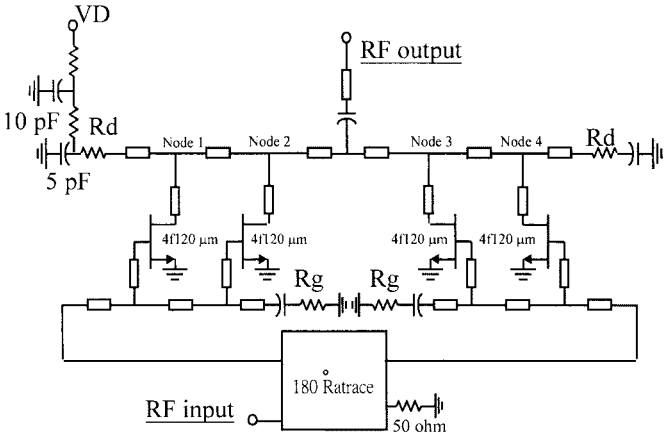

Fig. 1. Circuit schematic diagram of the broad-band MMIC distributed doubler.

This paper presents a MMIC pseudomorphic high electron-mobility transistor (pHEMT) balanced distributed frequency doubler to operate from 30- to 50-GHz output frequencies. By using a reduced-size broad-band 180° rat-race hybrid [15] in the balanced distributed doubler input port, the second harmonic signal will in-phase combine and fundamental and third harmonic signals will 180° out-of-phase cancel in the RF output port, also with a miniature chip size of 1.5 mm $\times$ 1 mm. The measured conversion loss is 5–7 dB from 30 to 50 GHz, while the fundamental and third harmonic suppressions are better than 13 and 25 dB, respectively.

II. Device Chracteristics and MMIC Fabrication

The MMIC distributed doubler were fabricated using a GaAs-based pHEMT MMIC foundry process provided by TRW Inc., Redondo Beach, CA [16]. The active device is a 0.15-μm gate-length pHEMT with a unit current gain frequency (f_T) and a maximum oscillation frequency $(f_{\max})$ of 81 and 120 GHz. The peak of transconductance and drain current at peak transconductance $(I_{\rm dsp})$ are 400 mS/mm and 200 mA/mm, respectively. The passive components include a GaAs thin-film resistor, metal–insulator–metal (MIM) capacitor, inductor, and via-hole through a 100-μm GaAs substrate. The entire chip is also protected by silicon–nitride passivation for reliability concern.

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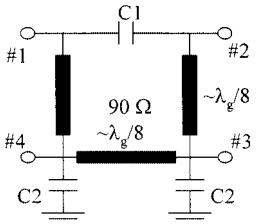


Fig. 2. Schematic diagram of the reduced-size 180° rat-race hybrid. The characteristic impedance and length of the transmission line are 90 Ω and $\lambda_g/8$. The value of the capacitors of $C1$ and $C2$ are both 0.12 pF.

III. Circuit Design

Fig. 1 is the schematic diagram of the 30–50-GHz balanced distributed doubler. The input fundamental signal is split into the two balanced ports with identical power and a phase difference of 180°, which travel down to the transmission lines, go through the active devices, and finally are absorbed by the gate termination resistor R_g. The forward second harmonic signals that pass the active devices then transmit to the output port and are in-phase combined. Some of the backward wave of the second harmonic signals will reflect to the circuit output due to the drain termination resistor. Based on the balanced structure, the second harmonic signal will be in-phase combined and the fundamental and odd harmonics signal will be antiphasal and cancelled in the circuit output port.

The doubler composes of four identical pHEMTs, each with a four-finger width and total gatewidth of 120 μm. In order to reduce the dc power consumption and generate the second harmonic signal, the transistors are biased near the pinchoff region, where the nonlinearity of transconductance versus gate-to-source voltage is used for frequency doubling. Microstrip lines are used to form the artificial gate and drain transmission lines, with in-phase for the second harmonic signals and 180° out-of-phase for canceling the fundamental signals and odd harmonics on the drain output port. In order to transmit the second harmonic signal in the drain line, the cutoff frequency of drain line need to be doubled for that of gate line. The drain-line length are determined by the design equations in [17] as

$$L_g = \frac{Z_g l_g}{v_g}$$
$$L_d = \frac{Z_d l_d}{v_d}$$
$$\omega_c = \frac{2}{\sqrt{L_g C_{gs}}} = \frac{2}{\sqrt{L_d C_{ds}}} \quad (1)$$

where L_g and L_d are per-unit-length inductance of gate and drain lines, l_g and l_d are the lengths of the unit gate and drain line sections and ω_c is the cutoff frequency of the gate and drain lines, Z_g and Z_d are the characteristic impedance of the gate and drain lines, C_{gs} and C_{ds} are the gate–source and drain–source capacitances, and v_g and v_d are the phase velocity of gate and drain lines, respectively.

The balanced distributed doubler employs common-source transistors, which form a lumped-element equivalent transmission line with a characteristic impedance Z_o at input RF frequency. The output drain line is also composed of two-section lumped-element equivalent transmission lines of

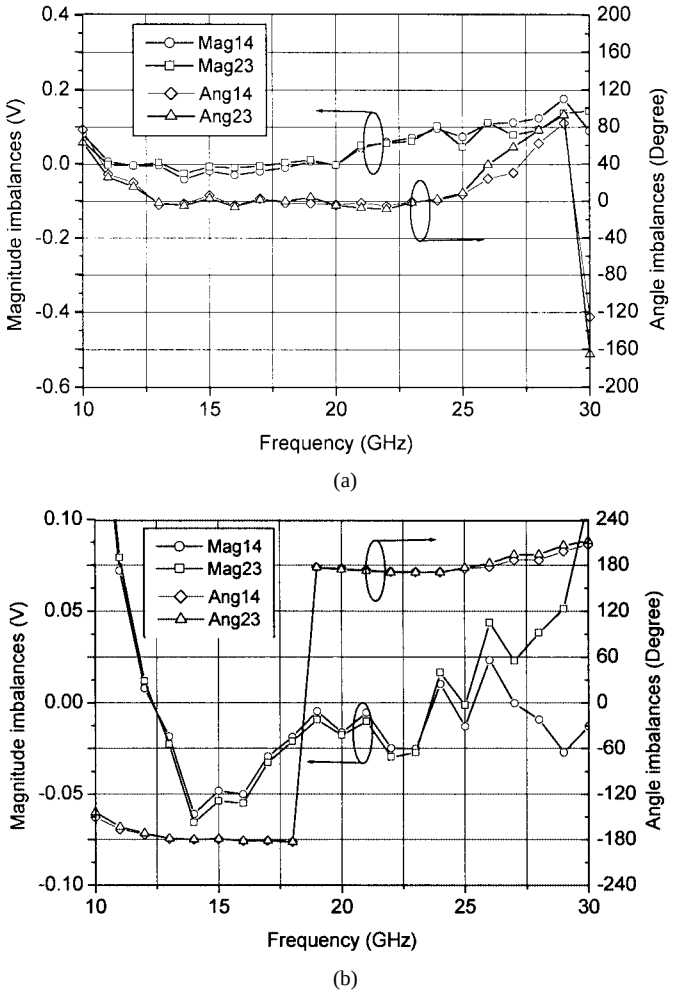
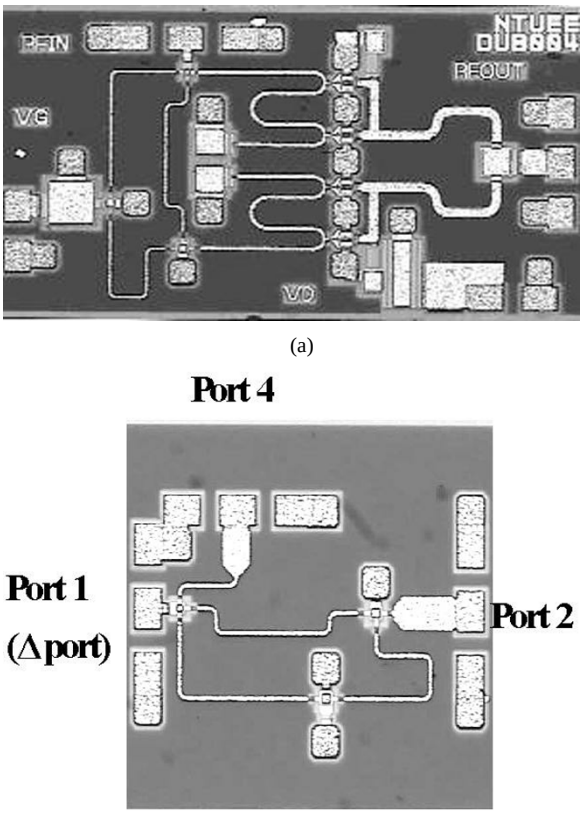


Fig. 3. Simulated: (a) second harmonic and (b) fundamental node voltage at the drain node 1–4 with an input power of 5 dBm and $V_{DS} = 3$ V, $V_{GS} = -0.8$ V.

impedance $2Z_o$ in the RF output frequency. The two sections of the balanced distributed doubler shown in Fig. 2 are selected to meet the specified bandwidth, chip area, and output power requirements. The 180° hybrid is a reduced-size rat-race hybrid design for wide bandwidth [15]. The schematic diagram is shown in Fig. 2. Three $\lambda_g/8$ wavelength microstrip transmission lines with a characteristic impedance of 90 Ω (width = 7 μm) and three MIM capacitors of 0.12 pF are used to implement the circuit. When the sum port (Fig. 2) is terminated with 50 Ω, the simulation results show that the insertion losses ($|S_{21}|$ and $|S_{41}|$) are 4 dB and another three-port return losses are better than −10 dB in the input RF frequencies from 15 to 25 GHz. The magnitude and phase imbalances of S_{21} and S_{41} of this hybrid are better than 1.2 dB and 10°, respectively.

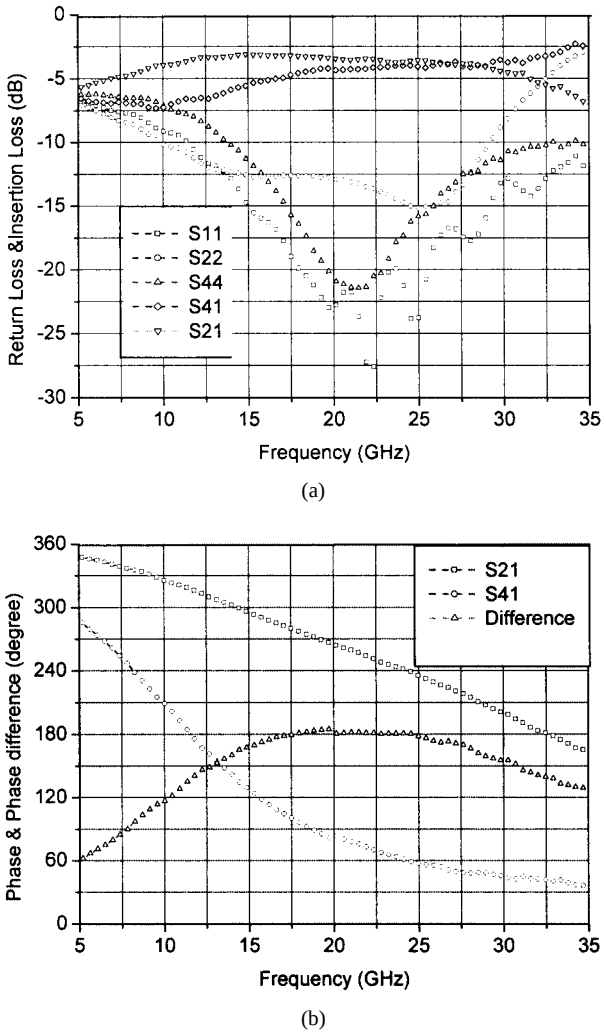
The input gate line from 15 to 25 GHz and output drain line from 30 to 50 GHz of the balanced distributed doubler are designed to provide broad-band operation. In order to reduce the overall chip size, the transistors biasing circuits are integrated with the output matching networks. The high-termination resistor R_d of the drain line is used to increase the backward wave of second harmonic signal to the drain line output and to match the second harmonic impedance. Unconditional stable operation is achieved by an additional *RC* parallel network shorted to the



(a)

(b)

Fig. 4. (a) Chip photograph of the broad-band MMIC distributed doubler with a chip size of 1.5×1 mm^2. (b) Chip photograph of the reduced-size 180° rat-race hybrid with a chip size of 1×0.5 mm^2.



(a)

(b)

Fig. 5. Measured characteristics of the reduced-size 180° rat-race hybrid. (a) Port return losses and insertion losses. (b) Phase and phase difference between these ports.

ground, in the output matching network, which also served for RF bypassing to desensitize the external biasing circuit.

The doubler performance is simulated via the harmonic-balance technique implemented in the commercial computer-aided design (CAD) software (LIBRA from HP-EESOF, Santa Rosa, CA). The nonlinear HEMT model used in the simulation is a Curtice cubic model provided by the foundry. The complete balanced distributed doubler with an ideal 180° hybrid is simulated first. The conversion loss is between 6–8 dB at output frequencies from 30 to 50 GHz with an input power level of 5 dBm. The input and output ports return losses are better than 7 dB, while the fundamental and third harmonic rejections are better than 20 and 40 dB, respectively. After replacing the reduced-size rat-race hybrid for the ideal 180° hybrid, it is observed that the conversion loss remains the same with the fundamental and third harmonic rejection down to 13 and 25 dB. This indicates that the phase and amplitude unbalances of the reduced-size rat-race hybrid do not impact the balanced distributed doubler conversion loss significantly.

In order to further investigate the features of the balanced doubler design, the node voltages defined in Fig. 1 are also studied via the nonlinear simulation. The simulated node voltages of the fundamental and second harmonic signals depicted in the schematic diagram in Fig. 1 are presented in Fig. 3. It is apparent that, for the second harmonic signals, the node voltage magnitude and phase imbalances (node1–node4 and node2–node3) are 0.01 V and 8° from 15 to 25 GHz. However, for the fundamental signals, the node voltage magnitude and phase imbalances (node1–node4 and node2 and node3) are 0.06 V and $180° \pm 5°$. Therefore, the second harmonic signals will be in-phase combined and the fundamental and third harmonic signals will be 180° out-of-phase and canceled at the output port.

Fig. 4(a) shows a photograph of the complete MMIC broad-band distributed doubler chip with a chip size of 1.5×1 mm^2. The reduced-size 180° rat-race hybrid is also placed on the same mask as a four-port test structure shown in Fig. 4(b), with a die size of 1×0.5 mm^2.

IV. Circuit Performance

Both the broad-band balanced distributed doubler chip and reduced-size rat-race hybrid test structure were measured via on-wafer probing. The rat-race hybrid was measured first and the results are presented in Fig. 5. All these port return losses are better than -12 dB and the insertion losses are 4.5 dB in the 17–28-GHz input RF frequency. The phase difference between

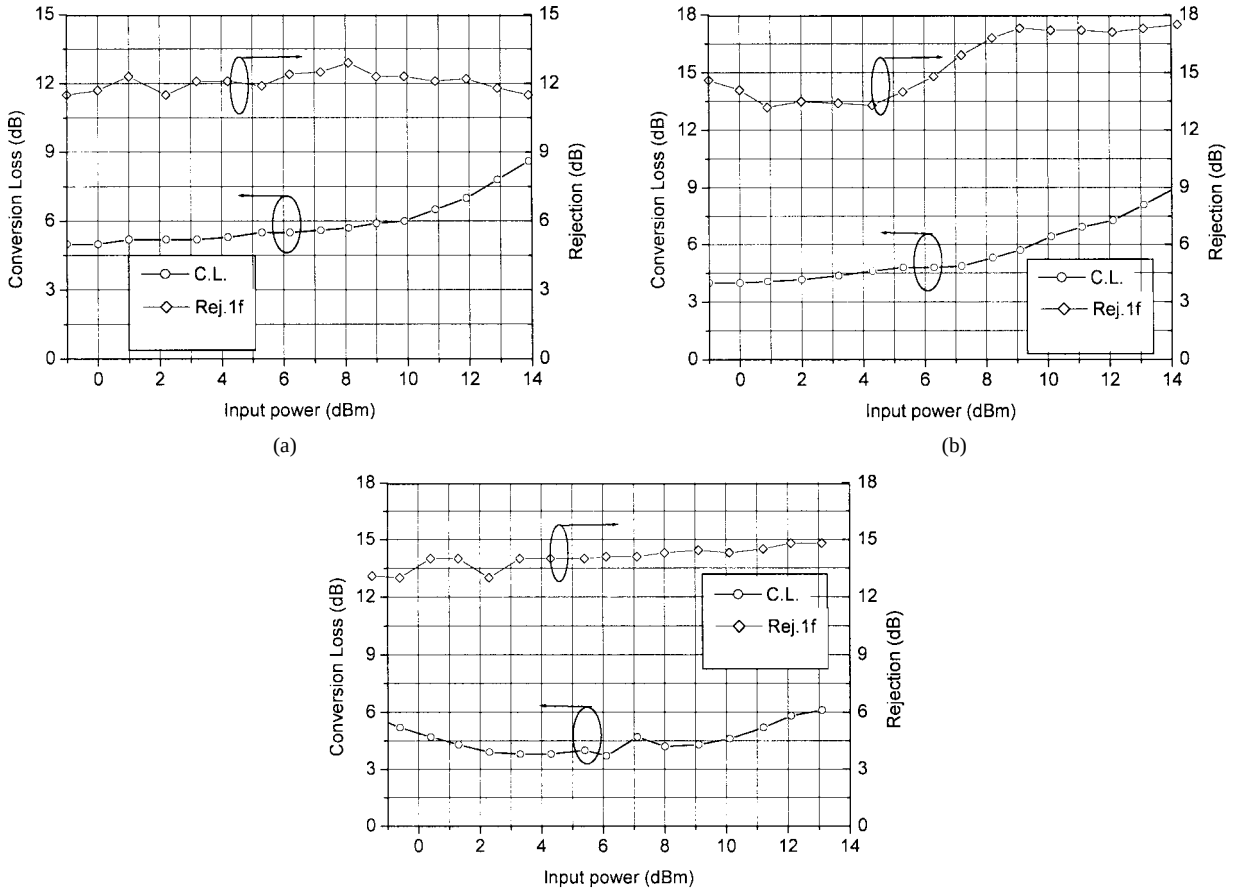


Fig. 6. Measured conversion loss, rejections, and output power for fundamental and second harmonic signals of the broad-band MMIC distributed doubler at input RF frequencies of: (a) 15 GHz, (b) 20 GHz, and (c) 25 GHz with $V_{\rm DS} = 3$ V and $V_{\rm GS} = -0.8$ V.

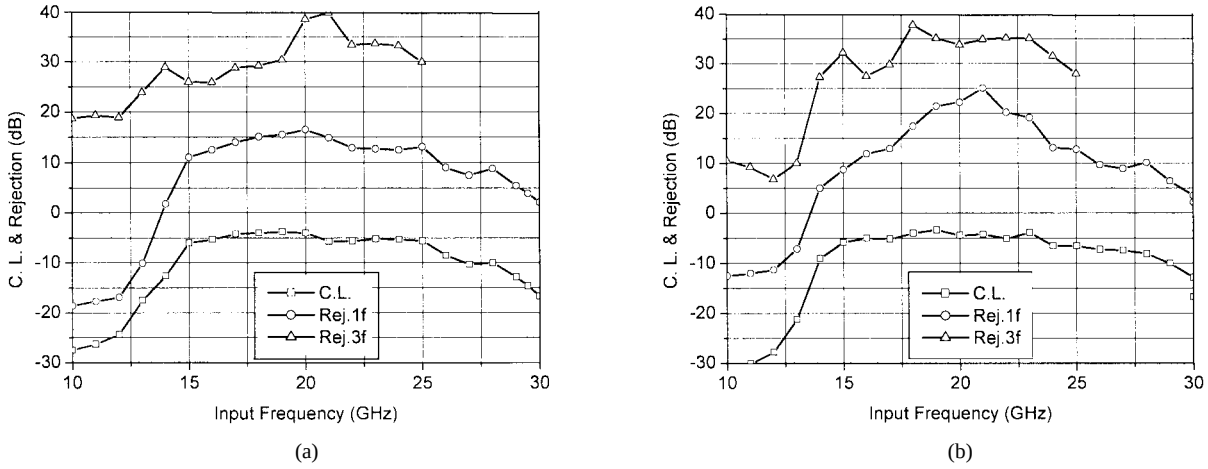


Fig. 7. Measured conversion loss and rejections of fundamental and third harmonic signal power level of the broad-band MMIC distributed doubler at RF input power levels of: (a) 5 dBm, and (b) 10 dBm with $V_{\rm DS} = 3$ V and $V_{\rm GS} = -0.8$ V.

two output ports are $180^\circ \pm 4^\circ$. The magnitude and phase imbalances of the hybrid are better than 1.5 dB and 8°.

In the measurement of the complete doubler, the transistors are all biased near the pinchoff region in the dc–*IV* curves. The conversion loss and the fundamental signal rejection versus input power from -1 to 14 dBm at input RF frequencies of 15, 20, and 25 GHz are plotted in Fig. 6 with $V_{\rm DS} = 3$ V, $V_{\rm GS} = -0.8$ V, and $I_{\rm DS} = 44$ mA. It is observed that, for an input power level above 5 dBm, the conversion performance becomes saturated. The conversion loss and fundamental signal rejection are 6 and 12 dB, respectively, at the input power of 5 dBm. The output 1-dB compression point of the second harmonic signal is 4 dBm. The measured conversion loss versus input frequency from 10 to 30 GHz with an input power level of 5 and 10 dBm are plotted in Fig. 7(a) and (b), respectively. The measured conversion loss is between 5–7 dB across 15–25-GHz input frequencies and demonstrated a broad-band frequency doubling performance. The fundamental

and third harmonic rejections versus input frequency were also presented in Fig. 7(a) and (b). The fundamental and third harmonic rejections are greater than 13 and 25 dB, respectively, covering the input frequencies from 15 to 25 GHz. Under a higher input RF power (10 dBm), the measured conversion loss is between 5–8 dB across 15–28 GHz. The fundamental and third harmonic rejections are better than 20 dB with an input power level 10 dBm from 19 to 23 GHz. Compared with the previously published results [6]–[18], this MMIC doubler demonstrated wide-band performance at low input RF power drive among those with MMW output frequencies. The conversion loss is relative low even though our design is without a buffer amplifier.

V. Conclusion

A compact and wide-band balanced distributed doubler using a reduced-size 180° rat-race hybrid has been described in this paper. Using the input matching circuit from 15 to 25 GHz and output matching circuit from 30 to 50 GHz, the balanced distributed doubler are designed to provided broad-band operation. The conversion loss is 5–7 dB and the fundamental and third harmonic rejections are better than 13 and 25 dB, respectively, at input frequencies from 15 to 25 GHz with a compact chip size of only 1.5 mm^2.

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